FIG. 1

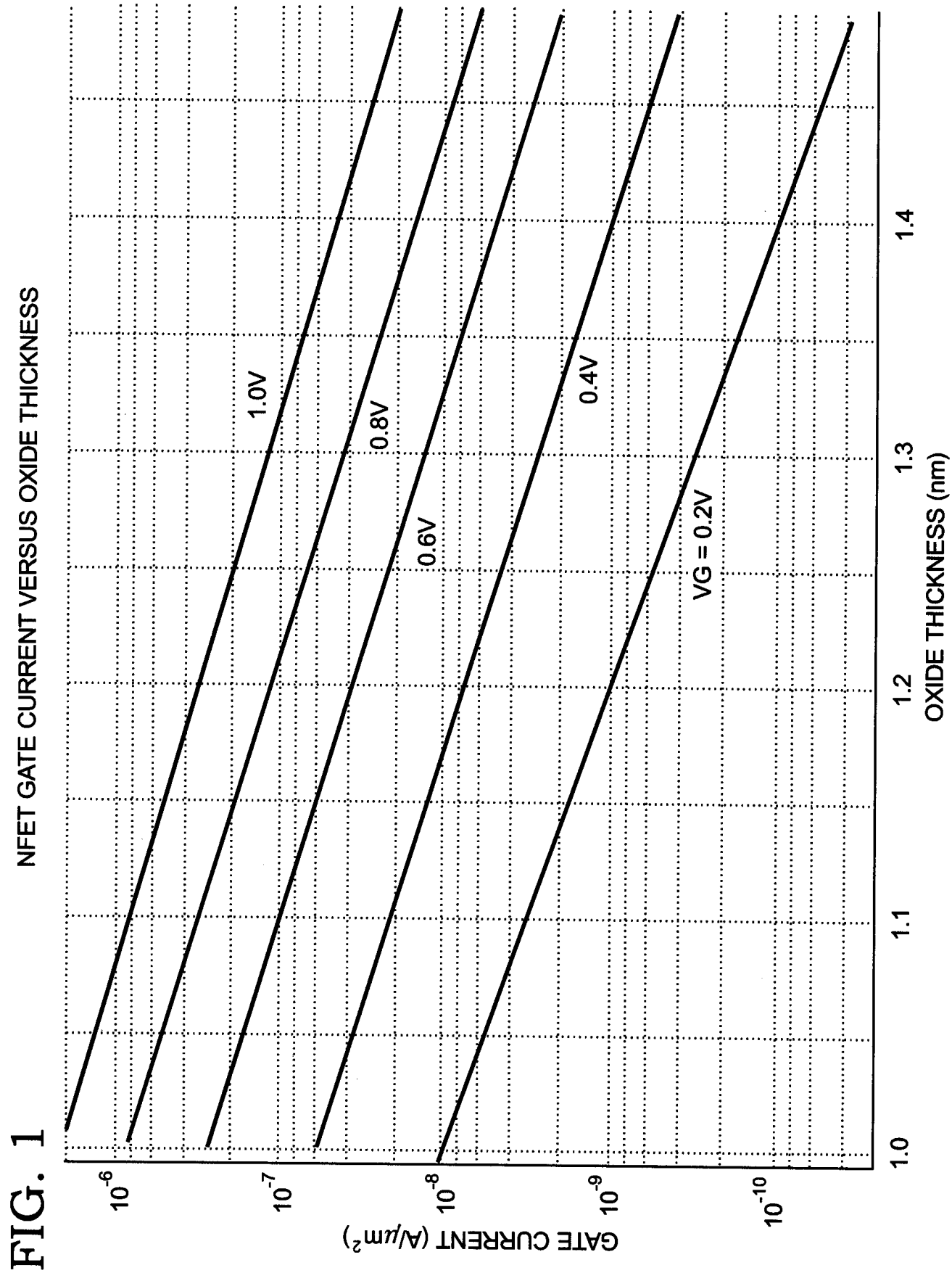

NFET GATE CURRENT VERSUS OXIDE THICKNESS
GATE CURRENT (A/μm²)
10^-6
10^-7
10^-8
10^-9
10^-10
1.0
1.1
1.2
1.3
1.4
OXIDE THICKNESS (nm)
1.0V
0.8V
0.6V
0.4V
VG = 0.2V

FIG. 2

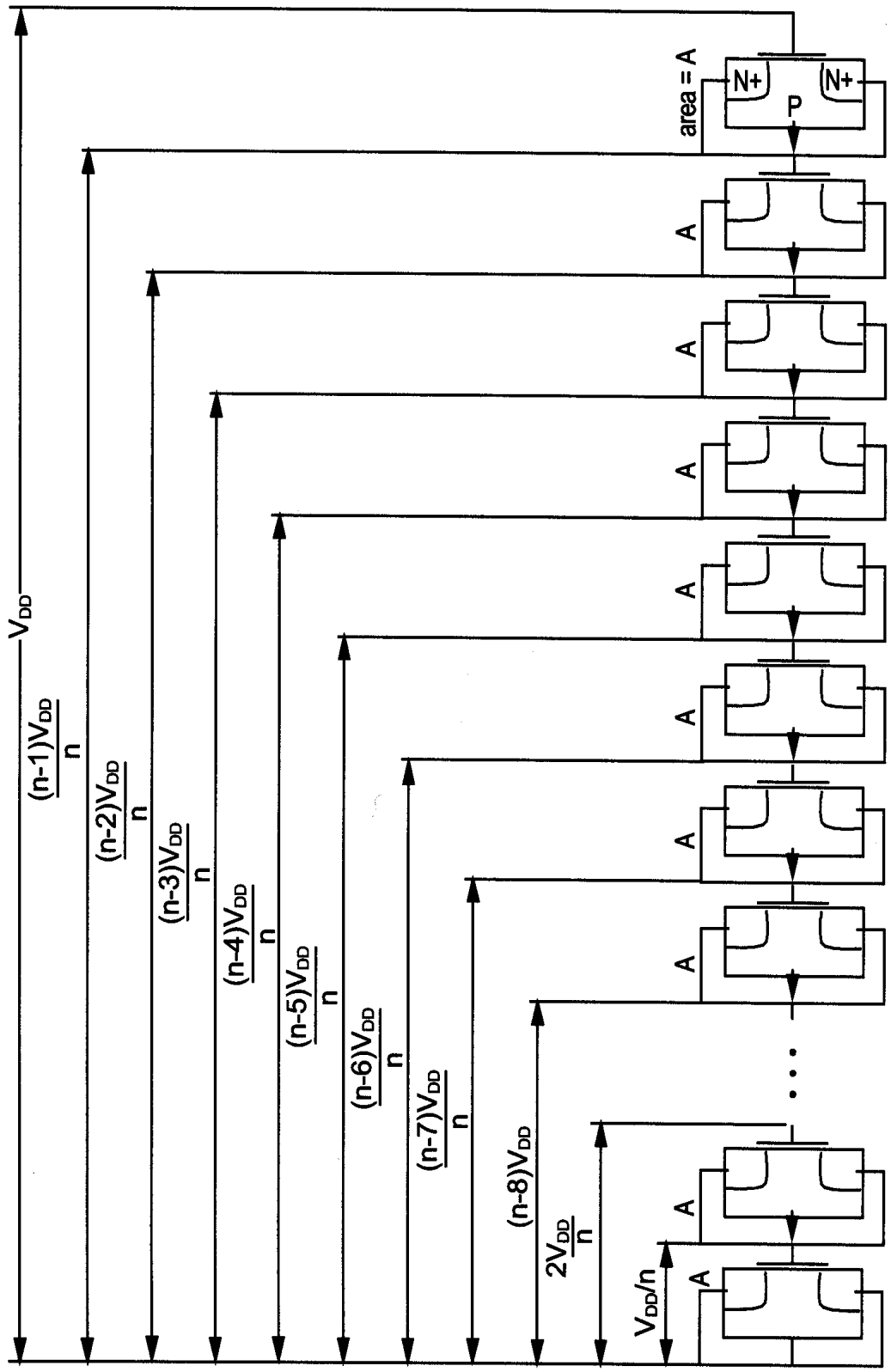

area = A
N+
N+
P
A
V_{DD}
$\frac{(n-1)V_{DD}}{n}$
$\frac{(n-2)V_{DD}}{n}$
$\frac{(n-3)V_{DD}}{n}$
$\frac{(n-4)V_{DD}}{n}$
$\frac{(n-5)V_{DD}}{n}$
$\frac{(n-6)V_{DD}}{n}$
$\frac{(n-7)V_{DD}}{n}$
$(n-8)V_{DD}$
$2\frac{V_{DD}}{n}$
V_{DD}/n

FIG. 3

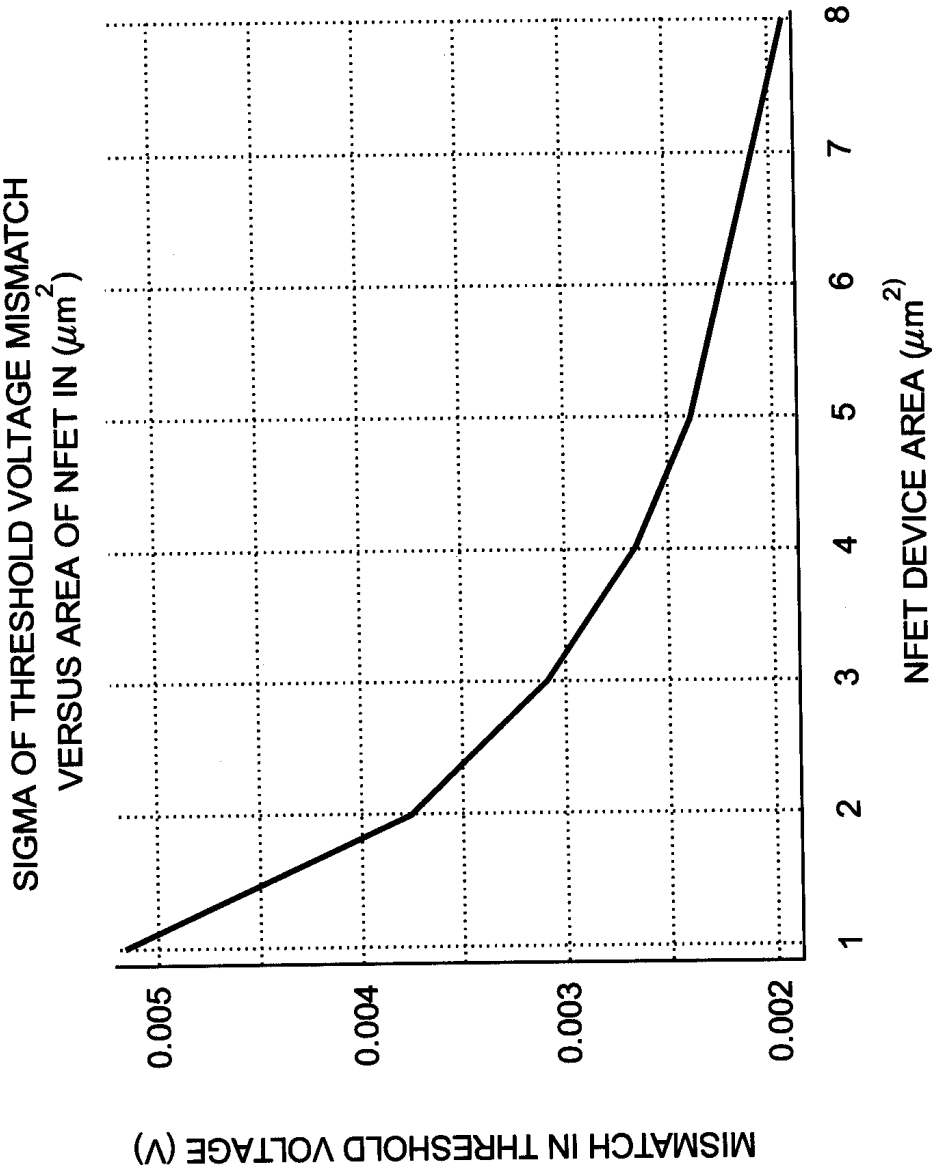

SIGMA OF THRESHOLD VOLTAGE MISMATCH
VERSUS AREA OF NFET IN (μm^2)
MISMATCH IN THRESHOLD VOLTAGE (V)
0.005
0.004
0.003
0.002
1
2
3
4
5
6
7
8
NFET DEVICE AREA (μm^2)

FIG. 4

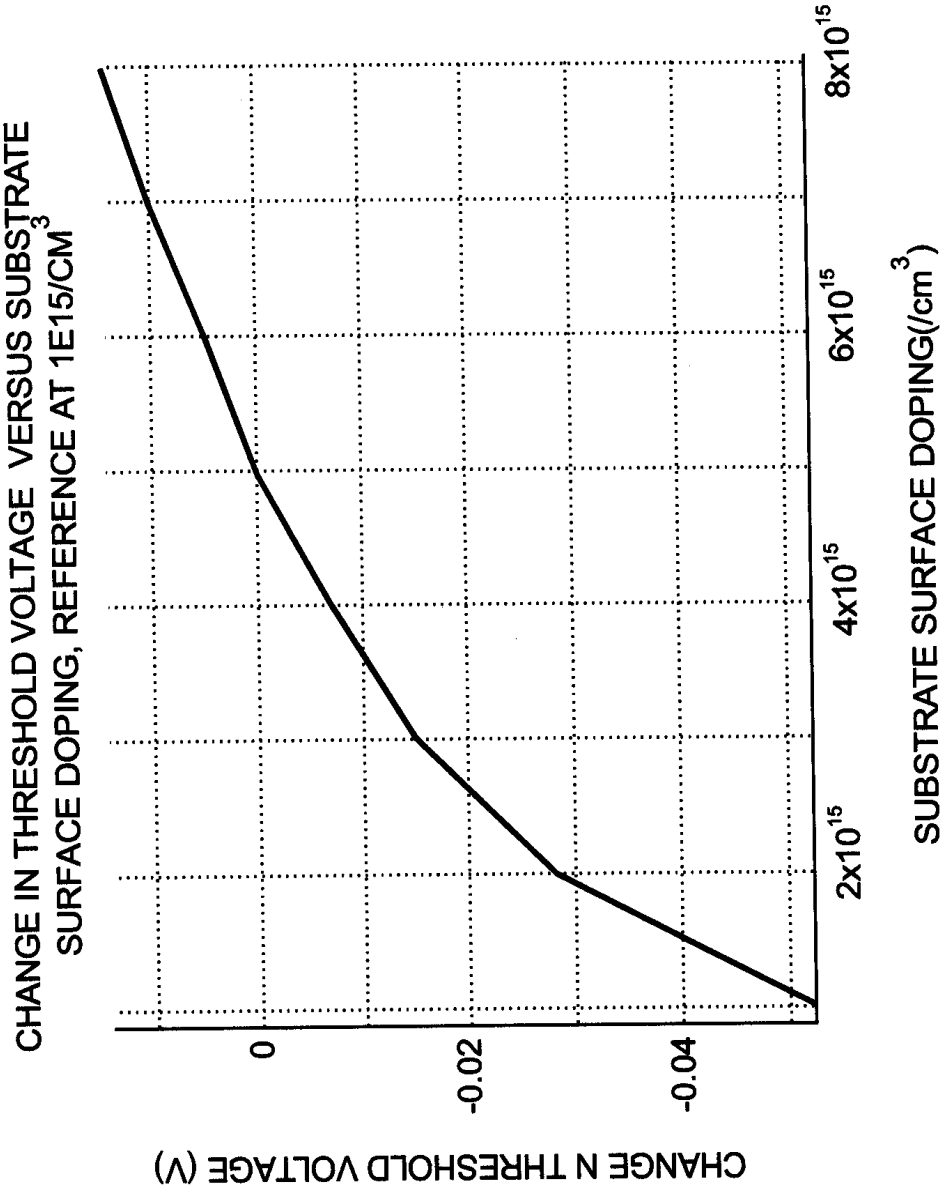

CHANGE IN THRESHOLD VOLTAGE VERSUS SUBSTRATE SURFACE DOPING, REFERENCE AT 1E15/CM3
CHANGE N THRESHOLD VOLTAGE (V)
0
-0.02
-0.04
2x10^15
4x10^15
6x10^15
8x10^15
SUBSTRATE SURFACE DOPING(/cm^3)

FIG. 5

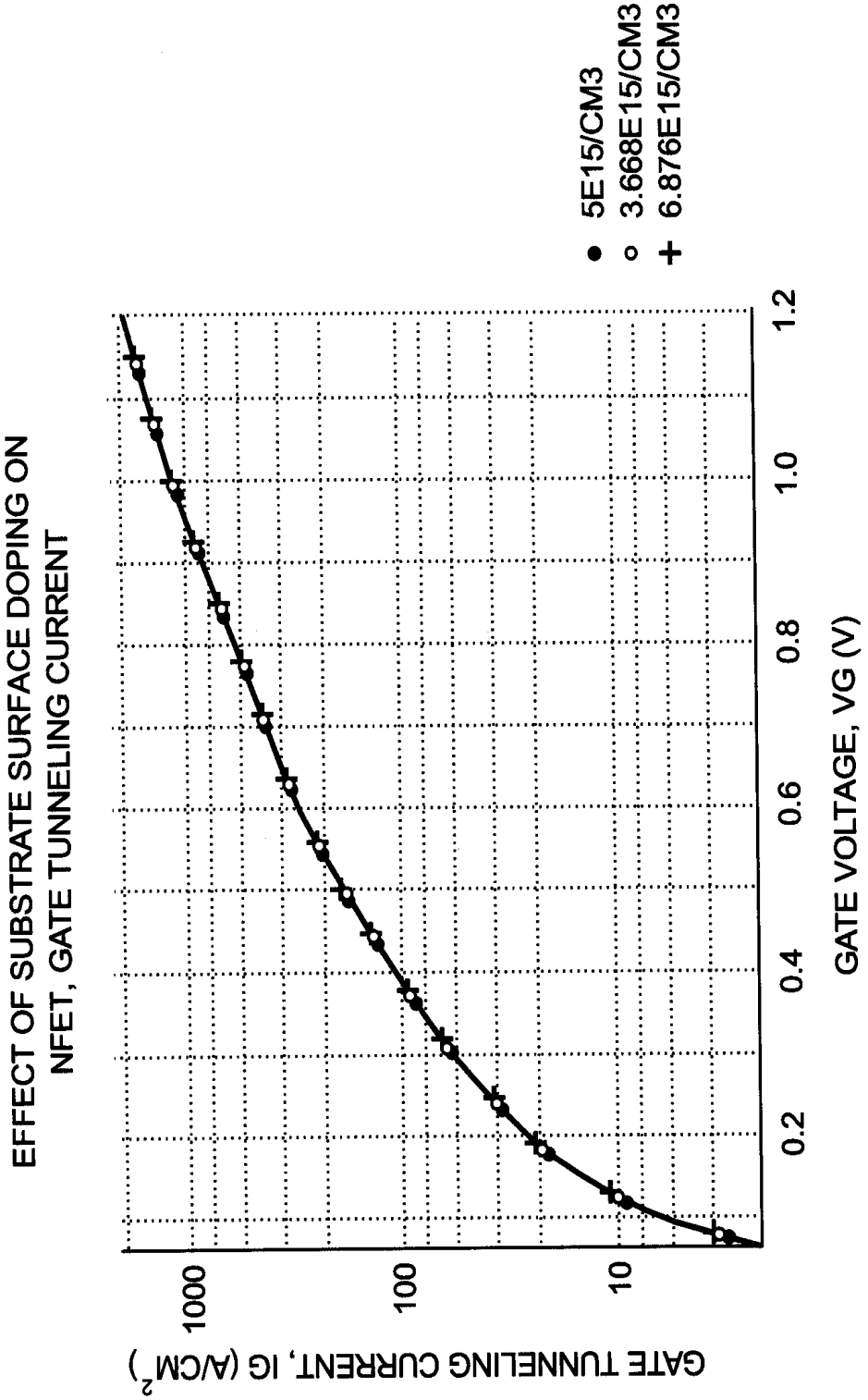

EFFECT OF SUBSTRATE SURFACE DOPING ON
NFET, GATE TUNNELING CURRENT
GATE TUNNELING CURRENT, IG (A/CM2)
1000
100
10
0.2
0.4
0.6
0.8
1.0
1.2
GATE VOLTAGE, VG (V)
5E15/CM3
3.668E15/CM3
6.876E15/CM3

FIG. 6

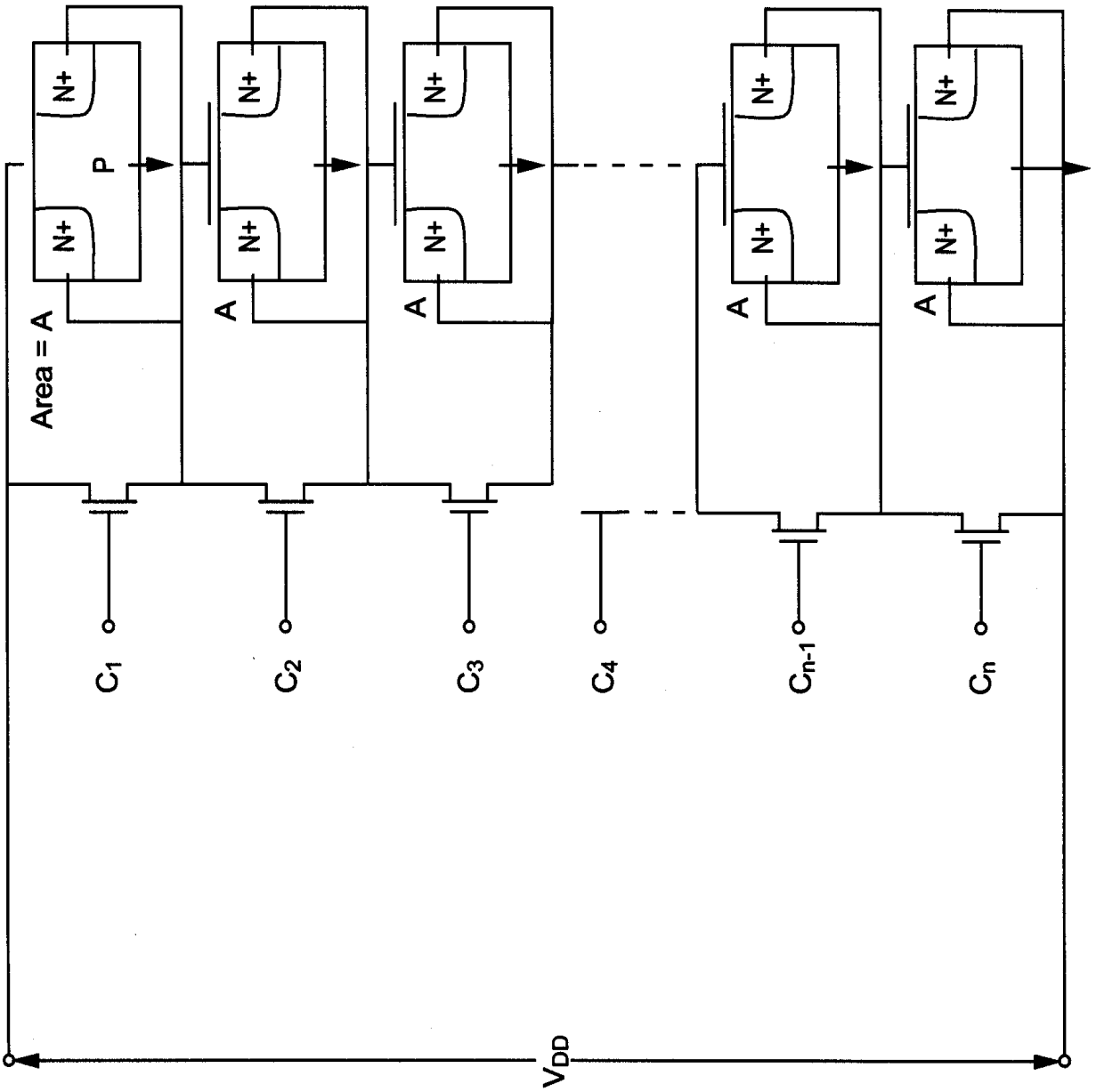


FIG. 7

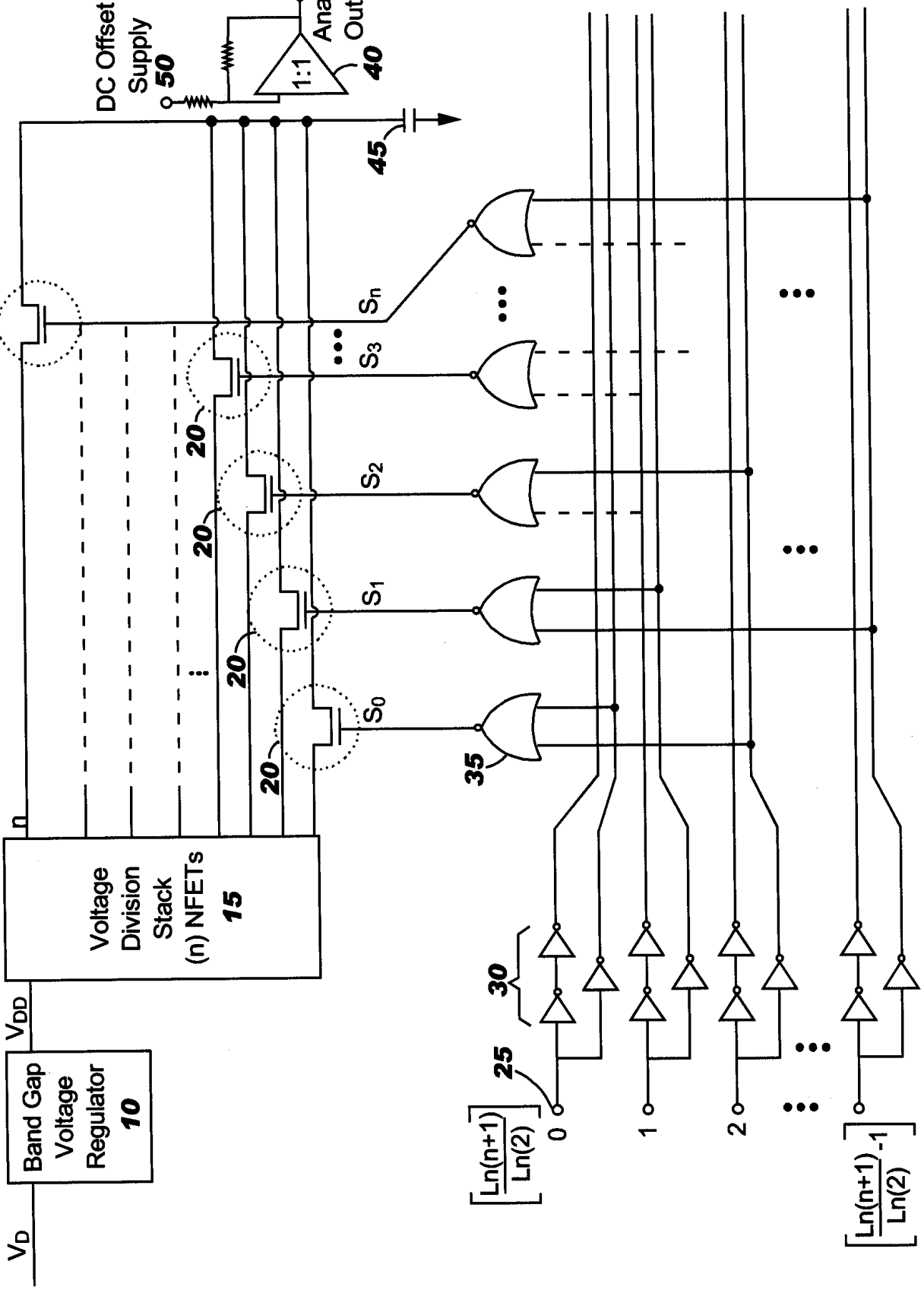
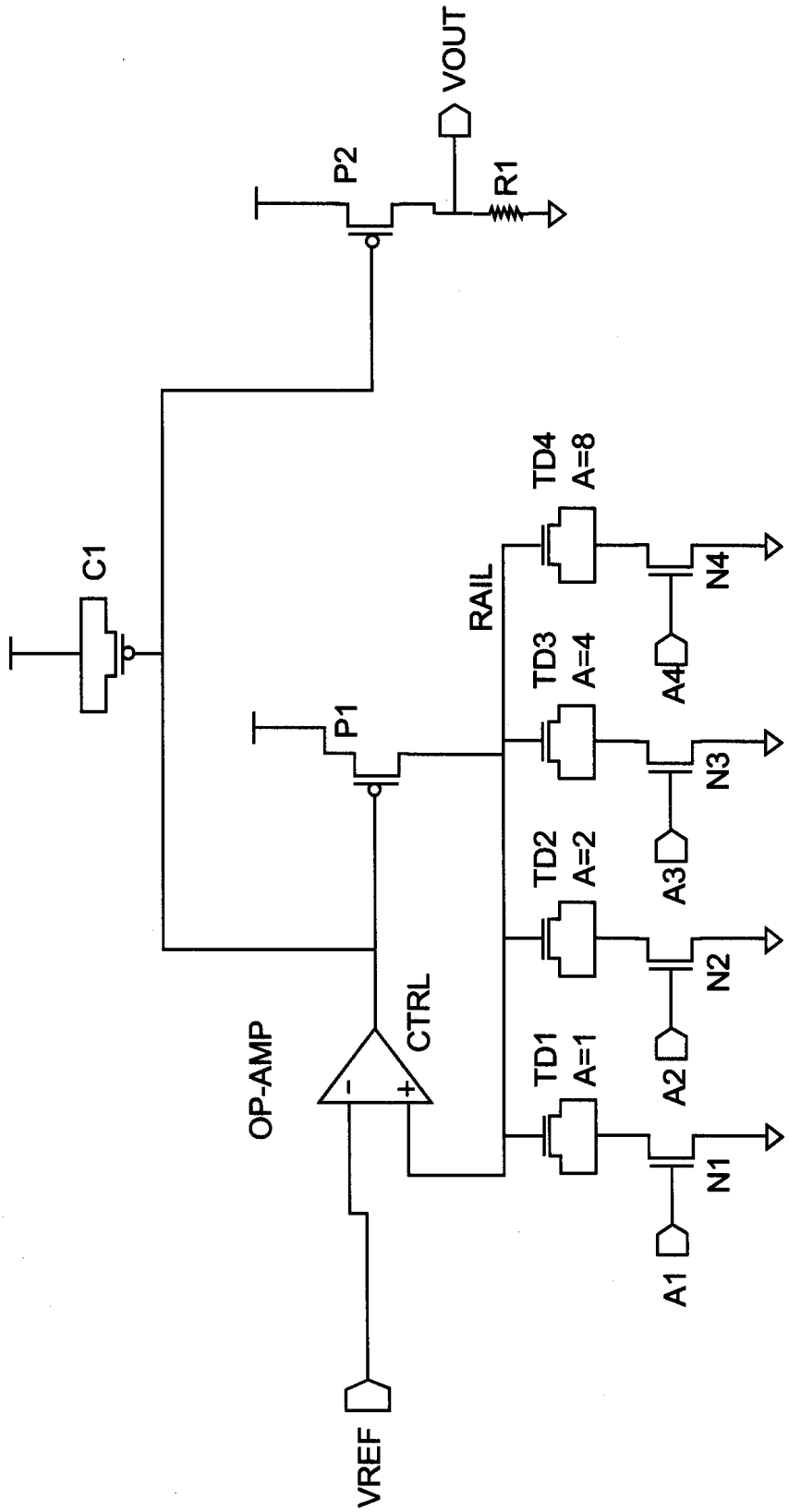

Band Gap Voltage Regulator 10
V_D
V_{DD}
Voltage Division Stack (n) NFETs 15
n
DC Offset Supply 50
1:1
Analog Output 40
45
20
S_n
S_3
S_2
S_1
S_0
35
30
25
$\left[\frac{Ln(n+1)}{Ln(2)}\right]$
0
1
2
$\left[\frac{Ln(n+1)}{Ln(2)}\right]$ -1

FIG. 8


VOUT
P2
R1
C1
TD4
A=8
RAIL
N4
A4
TD3
A=4
P1
N3
A3
TD2
A=2
N2
A2
CTRL
OP-AMP
TD1
A=1
N1
A1
VREF

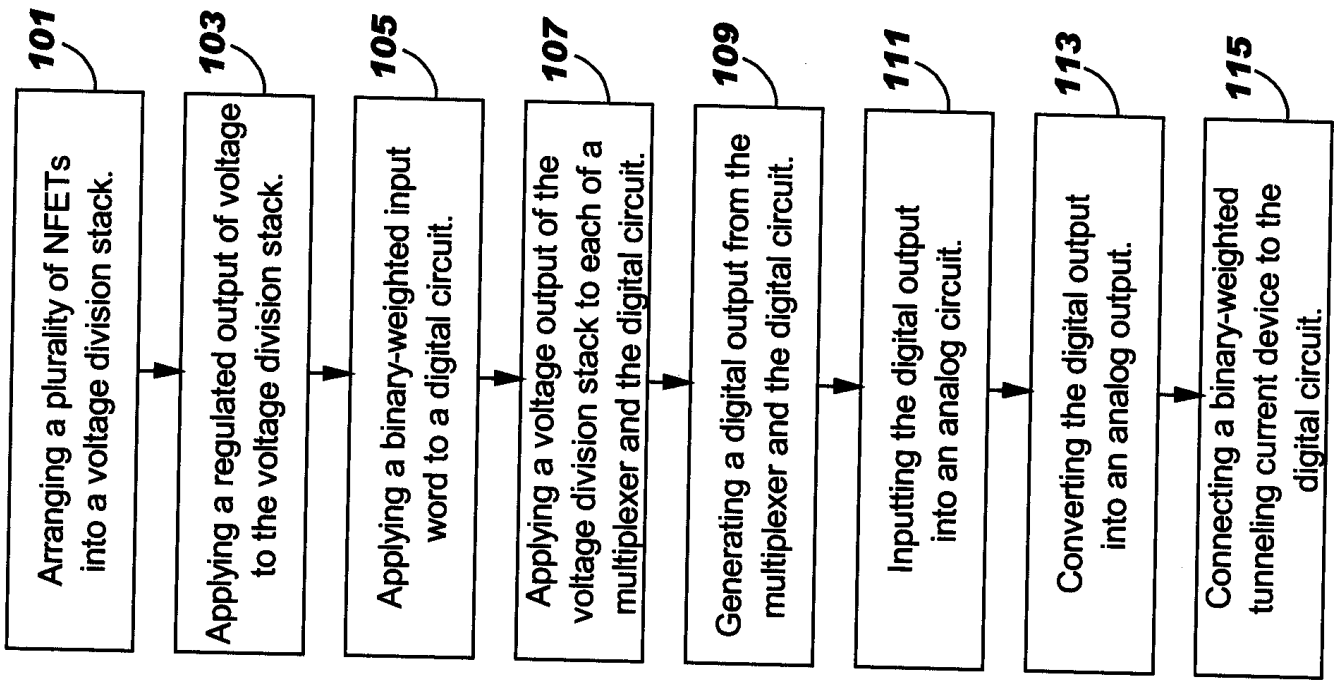

101
Arranging a plurality of NFETs into a voltage division stack.
103
Applying a regulated output of voltage to the voltage division stack.
105
Applying a binary-weighted input word to a digital circuit.
107
Applying a voltage output of the voltage division stack to each of a multiplexer and the digital circuit.
109
Generating a digital output from the multiplexer and the digital circuit.
111
Inputting the digital output into an analog circuit.
113
Converting the digital output into an analog output.
115
Connecting a binary-weighted tunneling current device to the digital circuit.

FIG. 9